PROLABS – QSFP-4x10G-AC7M-C

QSFP+ to 4 SFP+ Active Copper Cable Assembly

QSFP-4x10G-AC7M-C Overview

PROLABS's QSFP-4x10G-AC7M-C QSFP+ (Quad Small Form-factor Pluggable Plus) to 4 SFP+ Active Copper are suitable for very short distances and offer a highly cost-effective way to connect QSFP+ and SFP+ equipment. The direct-attach assemblies support 4 lanes of 10Gbps (40Gbps composite). This interconnect system is fully compliant with QSFP+ MSA and SFP+ MSA.

Product Features

- QSFP+ End: Compliant with QSFP+ MSA specifications
- SFP+ End: Compliant with SFP+ MSA specifications
- 4 independent duplex channels operating at 10Gbps,also support for 2.5Gbps,5Gbps data rates
- All-metal housing for superior EMI performance
- Single power supply 3.3V, low power consumption
- RoHS Compliance
- Operating temperature range: 0℃ to 70℃.

Applications

- 10Gigabit Ethernet
- Serial Data Transmission
- Networking
- Storage
- Fiber Channel

Ordering Information

Part Number	***Description***
QSFP-4x10G-AC7M-C	QSFP+ to 4 SFP+ Active Copper Cable Assembly, 7 Meter

General Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Bit Error Rate	*BER*			10^{-12}		
Operating Temperature	T_{OP}	0		70	℃	Case temperature
Storage Temperature	T_{STO}	– 40		85	℃	Ambient temperature
Input Voltage	V_{CC}	3	3.3	3.6	V	
Maximum Voltage	V_{MAX}	– 0.5		4	V	For electrical power interface

Cable Mechanical Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Wire Gauge			30AWG			
Cable Impedance	*Z*	95	100	105	Ohm	

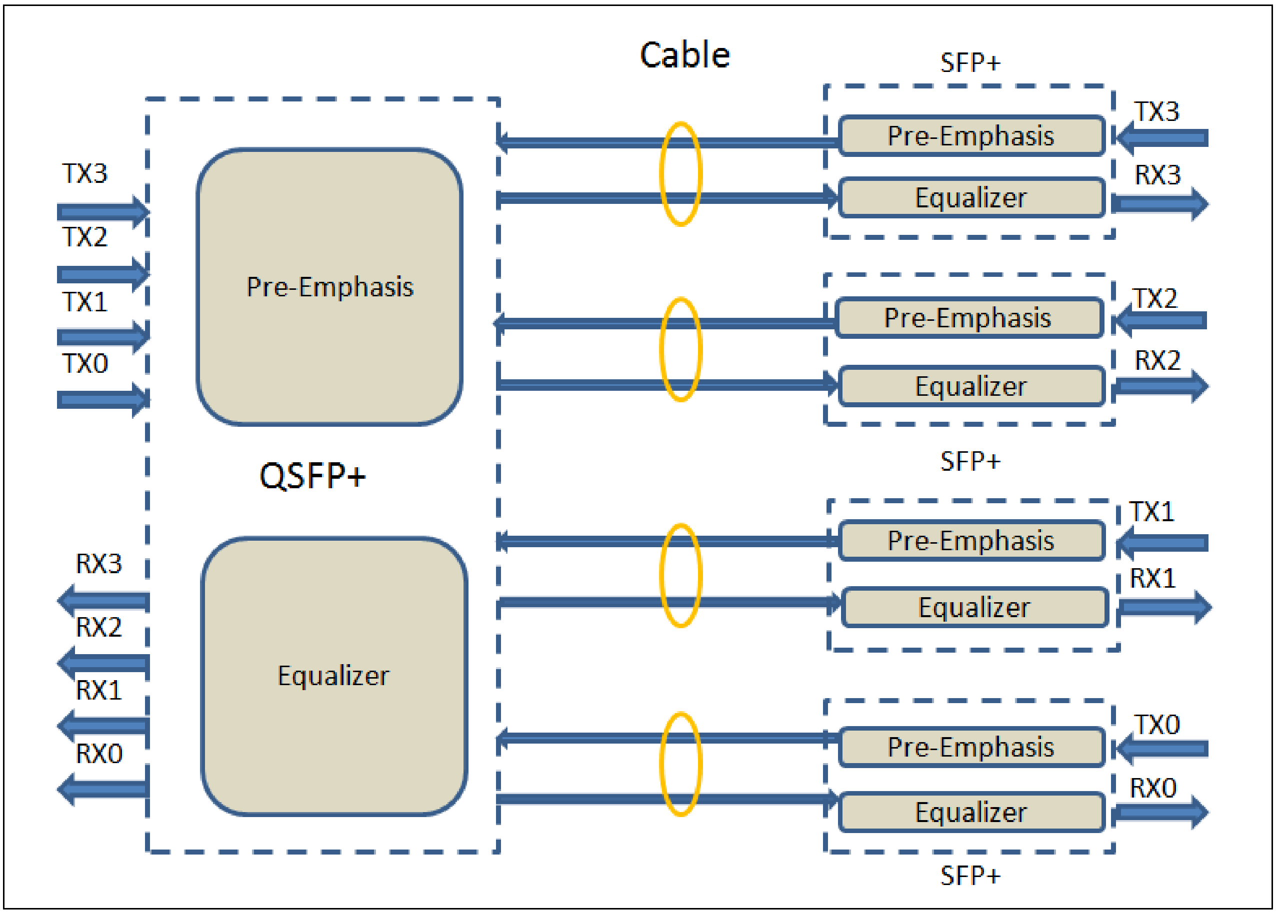
Electrical Input Requirements

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Data Rate Per Channel	*Dr*	2.5G		10.3G	GB/s	Non condensing
Differential Input Amplitude	$V_{IN\ PP}$	190		1600	mV	
Single Ended Voltage Tolerance	*V*	-0.3		3.8	V	

Electrical Output Requirements

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Data Rate Per Channel	*Dr*	2.5G		10.3G	GB/s	Non condensing
Differential Output Amplitude	$V_{OUT\ PP}$	350		900	mV	
Output Common-Mode Voltage	V_{CM-AC}		4.5		mV	
TX IDLE Output Voltage				30	mV	

Block Diagram of Transceiver



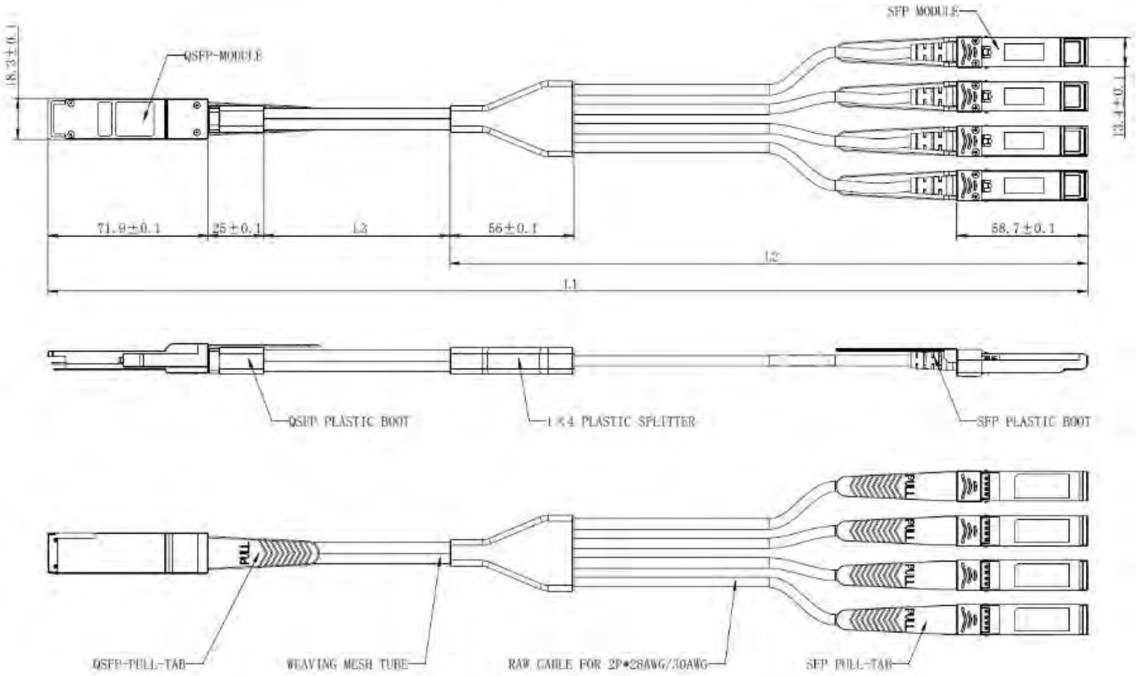
The transmitter side accepts electrical input signals. All input data signals are differential LVPECL or CML logic and they are internally terminated. The parallel input electrical signal first is processed via the Pre-Emphasis.

At the receiver side, the parallel electrical signals are recovered via Equalizer. The outputs electrical signals of receive side are voltage compatible with Current Mode Logic (CML) levels. All data signals are differential and support a data rate up to 10Gbps per channel.

All transmitter signals and receiver signals are AC coupled internally on both modules ends.

Active cable assembly has built-in MCU, offer a number of additional host-management capabilities. I2C (Inter-IC bus protocol) interface and on-board EEPROM features enable the host to detect or configure specific performance characteristics.

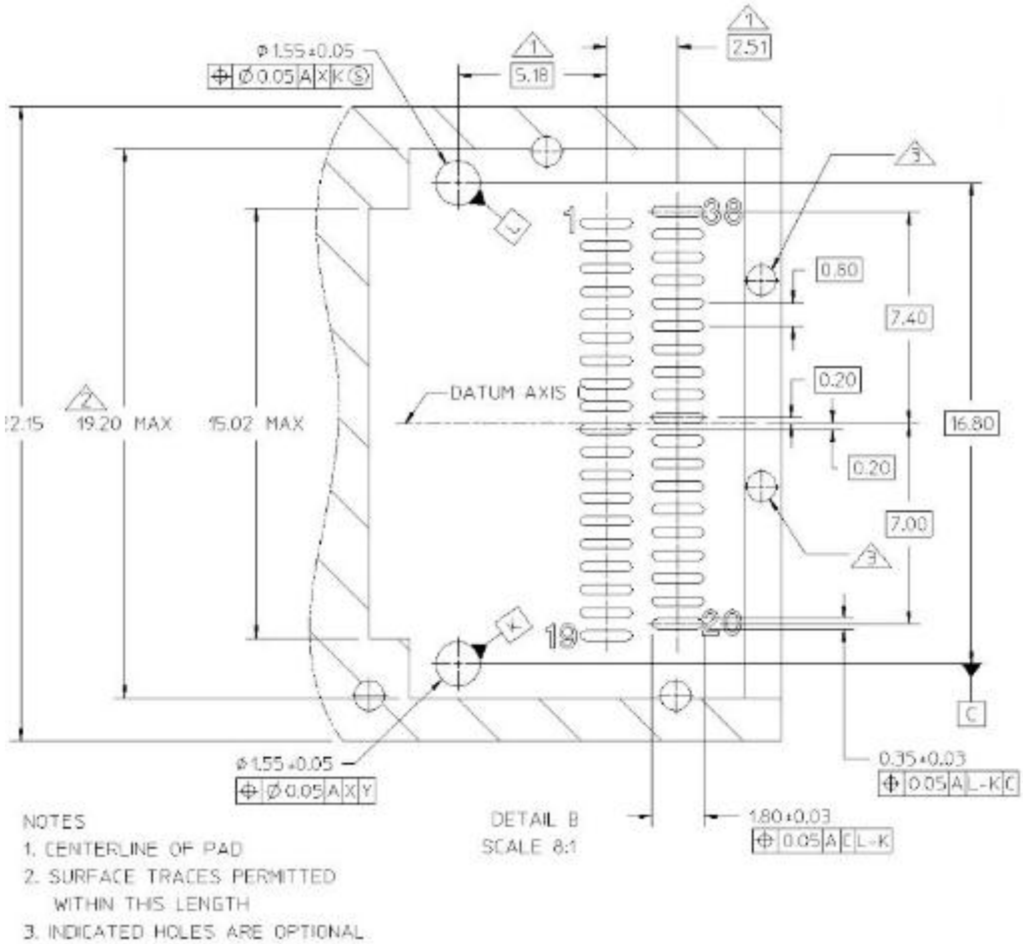
Outline Dimensions



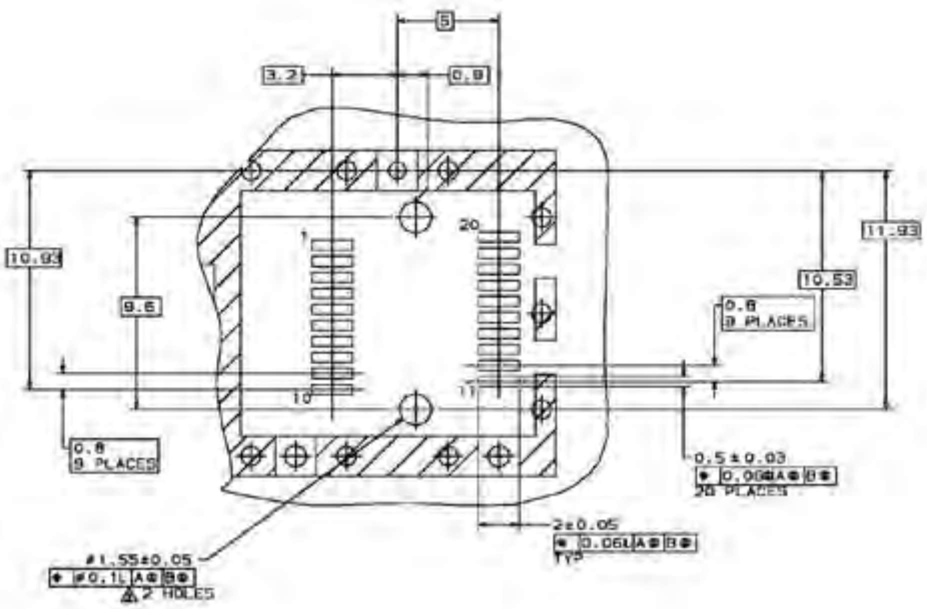
L1:7000mm±90mm

ALL DIMENSIONS （NOT INCLUDING THE LENGTH OF THE CABLE） ARE ±0.2mm
UNLESS OTHERWISE SPECIFIED
UNIT: mm

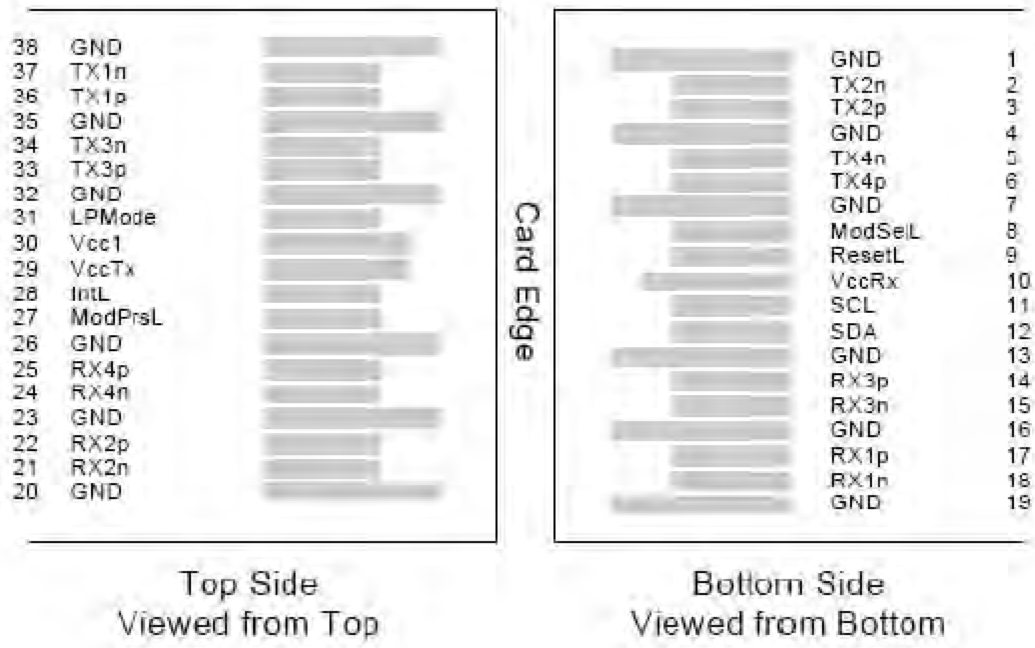
PCB Layout Recommendation (QSFP+ END)



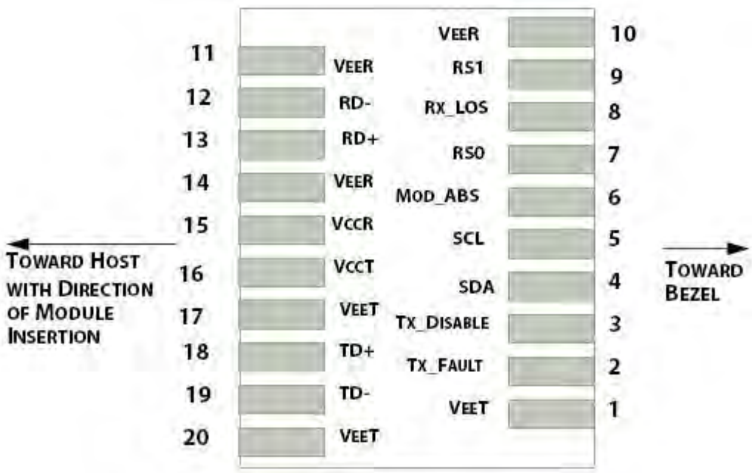
PCB Layout Recommendation (SFP+ END)



Electrical Pad Layout (QSFP+ END)



Electrical Pad Layout (SFP+ END)



Pin Assignment (QSFP+ END)

PIN #	Symbol	Description	Remarks
1	GND	Ground	
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	V_{cc} RX	+3.3V Power Supply Receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	
20	GND	Ground	
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	V_{cc} TX	+3.3V Power Supply transmitter	
30	V_{cc1}	+3.3V Power Supply	
31	LPMode	Low Power Mode	
32	GND	Ground	
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmiiter Inverted Data Input	
35	GND	Ground	
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmiiter Inverted Data Input	
38	GND	Ground	

Pin Assignment (SFP+ END)

PIN #	*Symbol*	*Description*	*Remarks*
1	V_{EET}	Transmitter ground (common with receiver ground)	
2	T_{FAULT}	Transmitter Fault.	
3	T_{DIS}	Transmitter Disable. Laser output disable on high or open	
4	SDA	Data line for serial ID	
5	SCL	Clock line for serial ID	
6	MOD_ABS	Module Absent. Grounded within the module	
7	RS0	No connection required	
8	LOS	Loss of Signal indication. Logic 0 indicates normal operation	
9	RS1	No connection required	
10	V_{EER}	Receiver ground (common with transmitter ground)	
11	V_{EER}	Receiver ground (common with transmitter ground)	
12	RD–	Receiver Inverted DATA out. AC coupled	
13	RD+	Receiver Non-inverted DATA out. AC coupled	
14	V_{EER}	Receiver ground (common with transmitter ground)	
15	V_{CCR}	Receiver power supply	
16	V_{CCT}	Transmitter power supply	
17	V_{EET}	Transmitter ground (common with receiver ground)	
18	TD+	Transmitter Non-Inverted DATA in. AC coupled	
19	TD–	Transmitter Inverted DATA in. AC coupled	
20	V_{EET}	Transmitter ground (common with receiver ground)	

References

1. Enhanced 8.5 and 10 Gigabit Small Form Factor Pluggable Module "SFP+" – SFF-8431
2. IEEE standard 802.3ae. IEEE Standard Department, 2008.
3. QSFP+ 10 Gbs 4X PLUGGABLE TRANSCEIVER –SFF-8436