

PROLABS – X4DACBLx-C

QSFP+ to 4 SFP+ Passive Copper Cable Assembly

X4DACBLx-C Overview

PROLABS's X4DACBLx-C QSFP+ (Quad Small Form-factor Pluggable Plus) to 4 SFP+ Copper direct-attach cables are suitable for very short distances and offer a highly cost-effective way to connect QSFP+ and SFP+ equipment. The direct-attach assemblies support 4 lanes of 10Gbps (40Gbps composite). This interconnect system is fully compliant with QSFP+ MSA and SFP+ MSA.

Product Features

- QSFP+ End: Compliant with QSFP+ MSA specifications
- SFP+ End: Compliant with SFP+ MSA specifications
- 4 independent duplex channels operating at 10Gbps, also support for 2.5Gbps, 5Gbps data rates
- AC coupled inputs and outputs
- 100 Ohm differential impedance
- All-metal housing for superior EMI performance
- Single power supply 3.3V, low power consumption
- RoHS Compliance
- Operating temperature range: 0°C to 70°C.

Applications

- 10Gigabit Ethernet
- Serial Data Transmission
- Networking
- Storage
- Fiber Channel

Ordering Information

Part Number	Description
X4DACBL1-C	QSFP+ to 4 SFP+ Direct Attach Copper Cable Assembly, 1 Meter
X4DACBL3-C	QSFP+ to 4 SFP+ Direct Attach Copper Cable Assembly, 3 Meter
X4DACBL5-C	QSFP+ to 4 SFP+ Direct Attach Copper Cable Assembly, 5 Meter

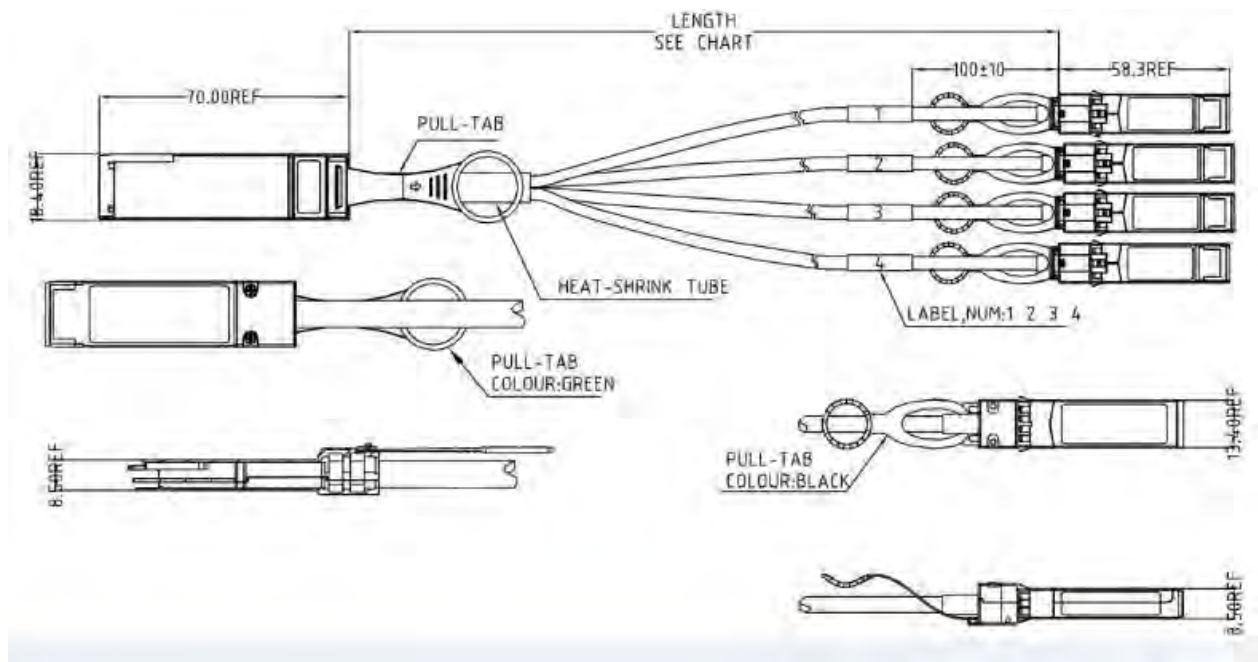
General Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Bit Error Rate	BER			10 ⁻¹²		
Operating Temperature	T _{OP}	0		70	°C	Case temperature
Storage Temperature	T _{STO}	- 40		85	°C	Ambient temperature
Input Voltage	V _{CC}	3	3.3	3.6	V	
Maximum Voltage	V _{MAX}	- 0.5		4	V	For electrical power interface

Cable Mechanical Specifications

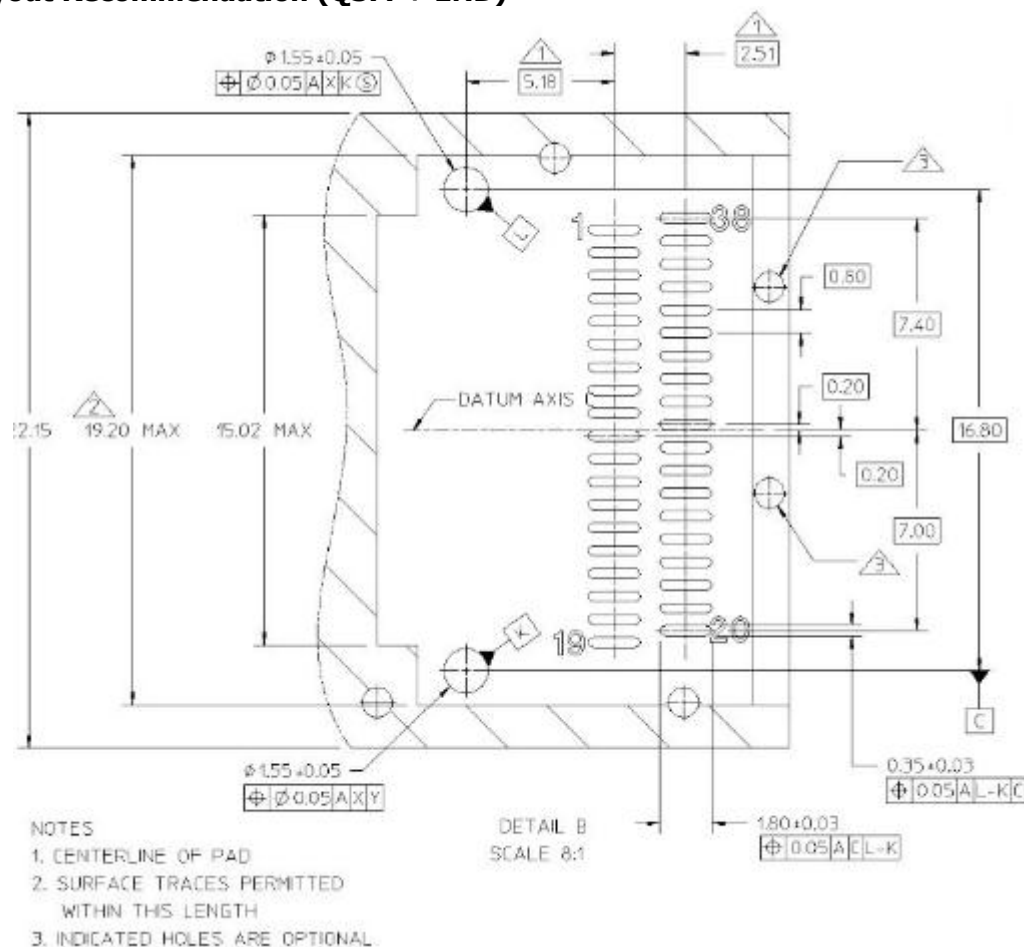
Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Wire Gauge			30AWG			
Cable Impedance	Z	95	100	105	Ohm	

Outline Dimensions



ALL DIMENSIONS ARE $\pm 0.2\text{mm}$ UNLESS OTHERWISE SPECIFIED
UNIT: mm

PCB Layout Recommendation (QSFP+ END)



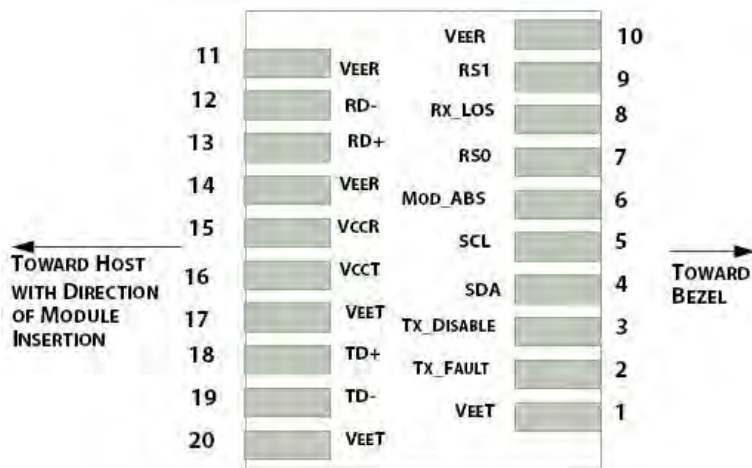
Technical drawing of a mechanical part, likely a bracket or plate, showing dimensions and tolerances. The drawing includes a top view and a side view. Key dimensions include overall width 11.93, overall height 10.93, and various hole positions and sizes. Tolerances are specified for several dimensions, such as 0.5 ± 0.03 and 1.55 ± 0.05 . Surface finish symbols are present on several surfaces.

The diagram illustrates the pin configuration for the top and bottom sides of the card edge connector. The top side (viewed from top) shows pins 38 to 20, and the bottom side (viewed from bottom) shows pins 1 to 19. The card edge is labeled 'Card Edge'.

Pin Number	Signal Name
38	GND
37	TX1n
36	TX1p
35	GND
34	TX3n
33	TX3p
32	GND
31	LPMode
30	Vcc1
29	VccTx
28	IntL
27	ModPrsL
26	GND
25	RX4p
24	RX4n
23	GND
22	RX2p
21	RX2n
20	GND

Pin Number	Signal Name
1	GND
2	TX2n
3	TX2p
4	GND
5	TX4n
6	TX4p
7	GND
8	ModSelL
9	ResetL
10	VccRx
11	SCL
12	SDA
13	GND
14	RX3p
15	RX3n
16	GND
17	RX1p
18	RX1n
19	GND

Electrical Pad Layout (SFP+ END)



Pin Assignment (QSFP+ END)

PIN #	Symbol	Description	Remarks
1	GND	Ground	
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	V _{cc} RX	+3.3V Power Supply Receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	
20	GND	Ground	
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	V _{cc} TX	+3.3V Power Supply transmitter	
30	V _{cc1}	+3.3V Power Supply	
31	LPMode	Low Power Mode	

32	GND	Ground
33	Tx3p	Transmitter Non-Inverted Data Input
34	Tx3n	Transmitter Inverted Data Input
35	GND	Ground
36	Tx1p	Transmitter Non-Inverted Data Input
37	Tx1n	Transmitter Inverted Data Input
38	GND	Ground

Pin Assignment (SFP+ END)

PIN #	Symbol	Description	Remarks
1	V _{EET}	Transmitter ground (common with receiver ground)	
2	T _{FAULT}	Transmitter Fault.	
3	T _{DIS}	Transmitter Disable. Laser output disable on high or open	
4	SDA	Data line for serial ID	
5	SCL	Clock line for serial ID	
6	MOD_ABS	Module Absent. Grounded within the module	
7	RS0	No connection required	
8	LOS	Loss of Signal indication. Logic 0 indicates normal operation	
9	RS1	No connection required	
10	V _{EER}	Receiver ground (common with transmitter ground)	
11	V _{EER}	Receiver ground (common with transmitter ground)	
12	RD-	Receiver Inverted DATA out. AC coupled	
13	RD+	Receiver Non-inverted DATA out. AC coupled	
14	V _{EER}	Receiver ground (common with transmitter ground)	
15	V _{CCR}	Receiver power supply	
16	V _{CCT}	Transmitter power supply	
17	V _{EET}	Transmitter ground (common with receiver ground)	
18	TD+	Transmitter Non-Inverted DATA in. AC coupled	
19	TD-	Transmitter Inverted DATA in. AC coupled	
20	V _{EET}	Transmitter ground (common with receiver ground)	

References

- Enhanced 8.5 and 10 Gigabit Small Form Factor Pluggable Module "SFP+" – SFF-8431
- IEEE standard 802.3ae. IEEE Standard Department, 2008.
- QSFP+ 10 Gbs 4X PLUGGABLE TRANSCEIVER –SFF-8436